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(54) SINGLE SUBSTRATE CAMERA DEVICE WITH CMOS IMAGE SENSOR

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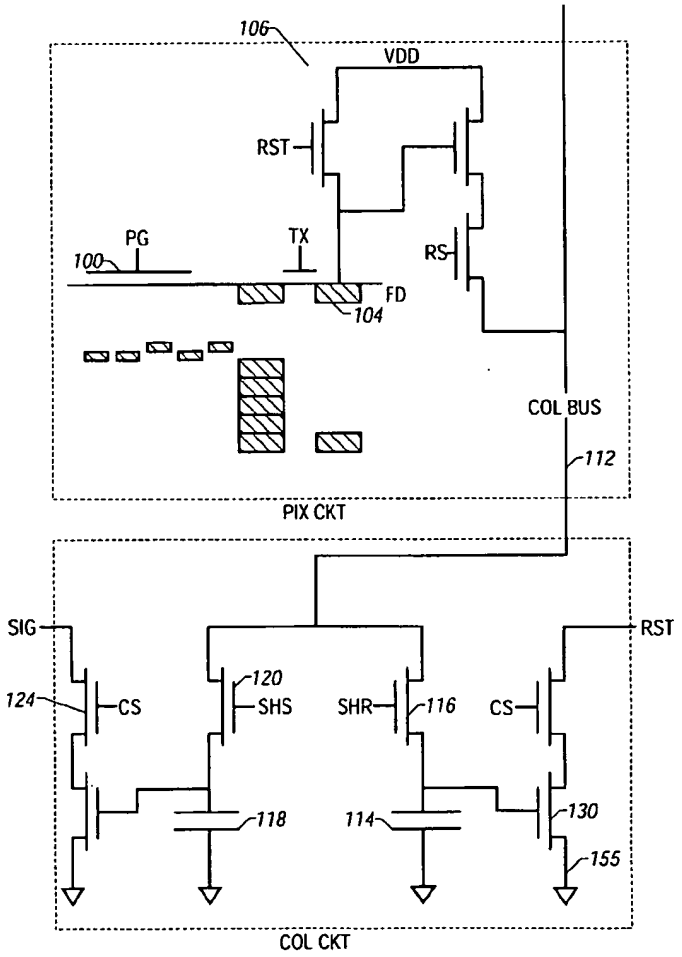
(57) ABSTRACT

Single substrate device is formed to have an image acquisition device and a controller. The controller on the substrate controls the system operation.



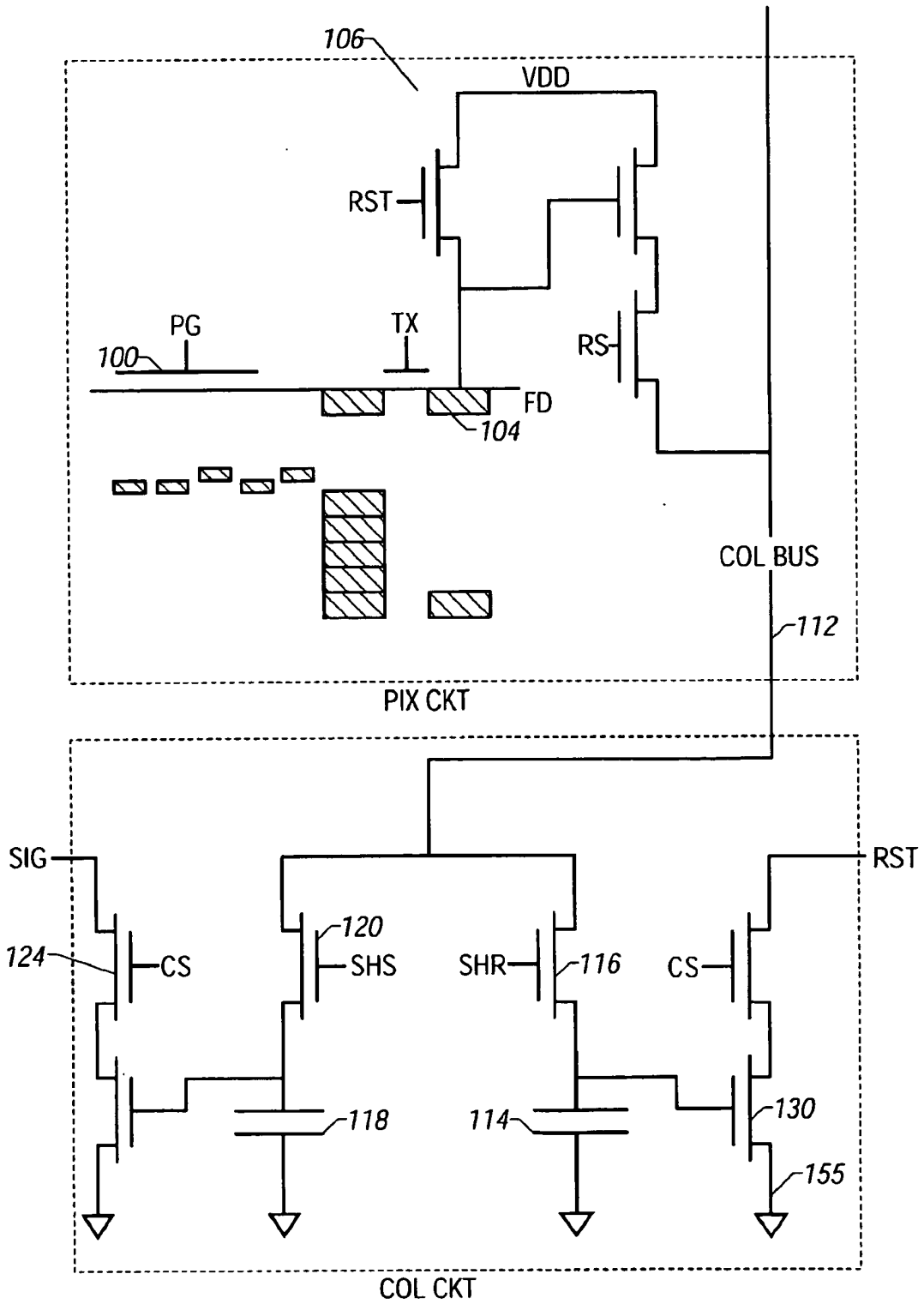

106
VDD
RST
PG
TX
RS
100
FD
104
COL BUS
112
PIX CKT
SIG
RST
124
CS
120
SHS
SHR
116
CS
118
114
130
155
COL CKT

FIG. 1

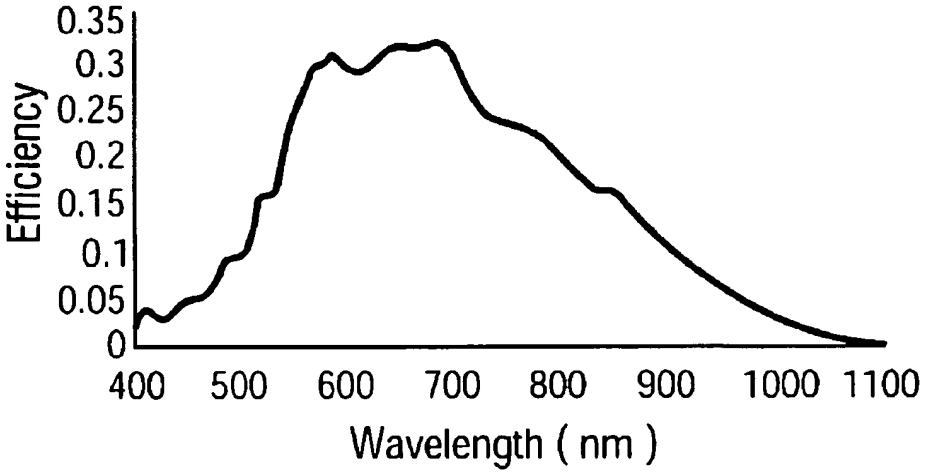

0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
Efficiency
400
500
600
700
800
900
1000
1100
Wavelength (nm)

FIG. 2

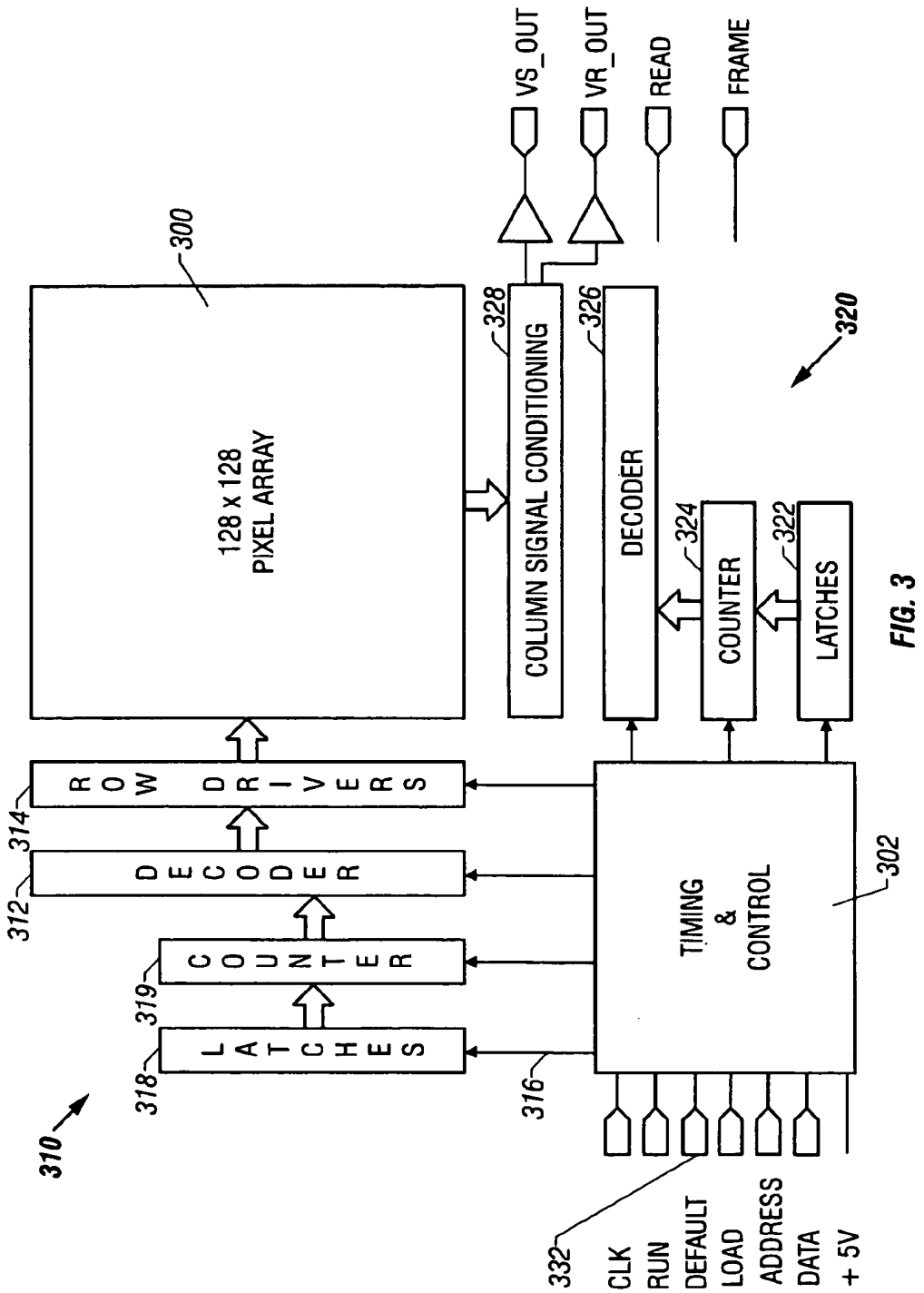

VS_OUT
VR_OUT
READ
FRAME
300
128 x 128
PIXEL ARRAY
328
COLUMN SIGNAL CONDITIONING
326
DECODER
320
324
COUNTER
322
LATCHES
ROW DRIVERS
314
DECODER
312
COUNTER
319
LATCHES
318
310
316
TIMING
&
CONTROL
302
332
CLK
RUN
DEFAULT
LOAD
ADDRESS
DATA
+ 5V

FIG. 3

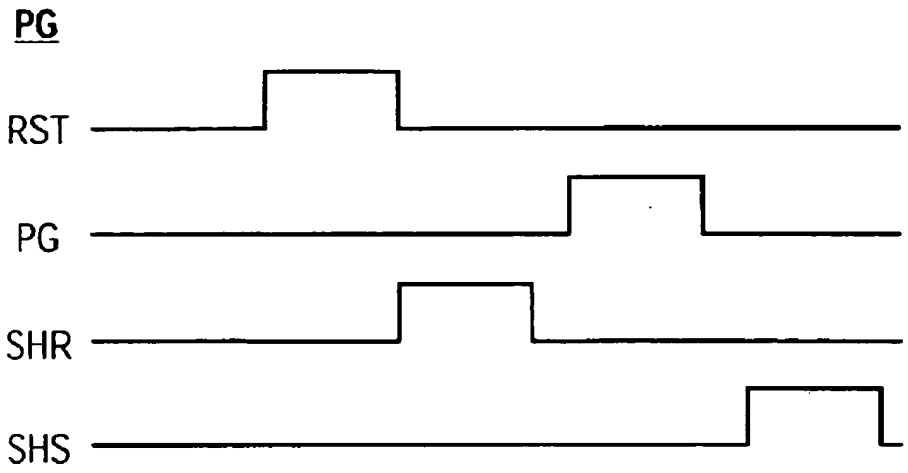


FIG. 4A

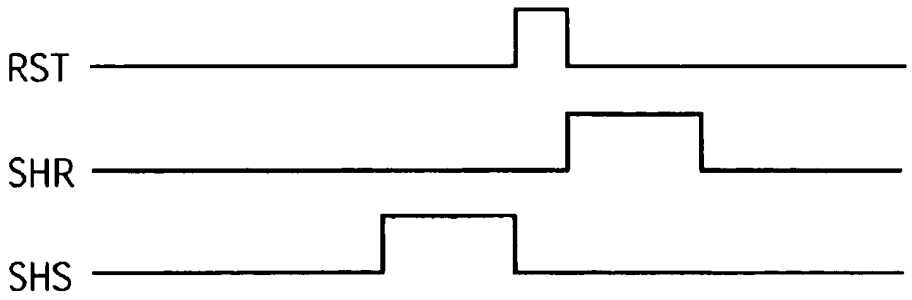


FIG. 4B

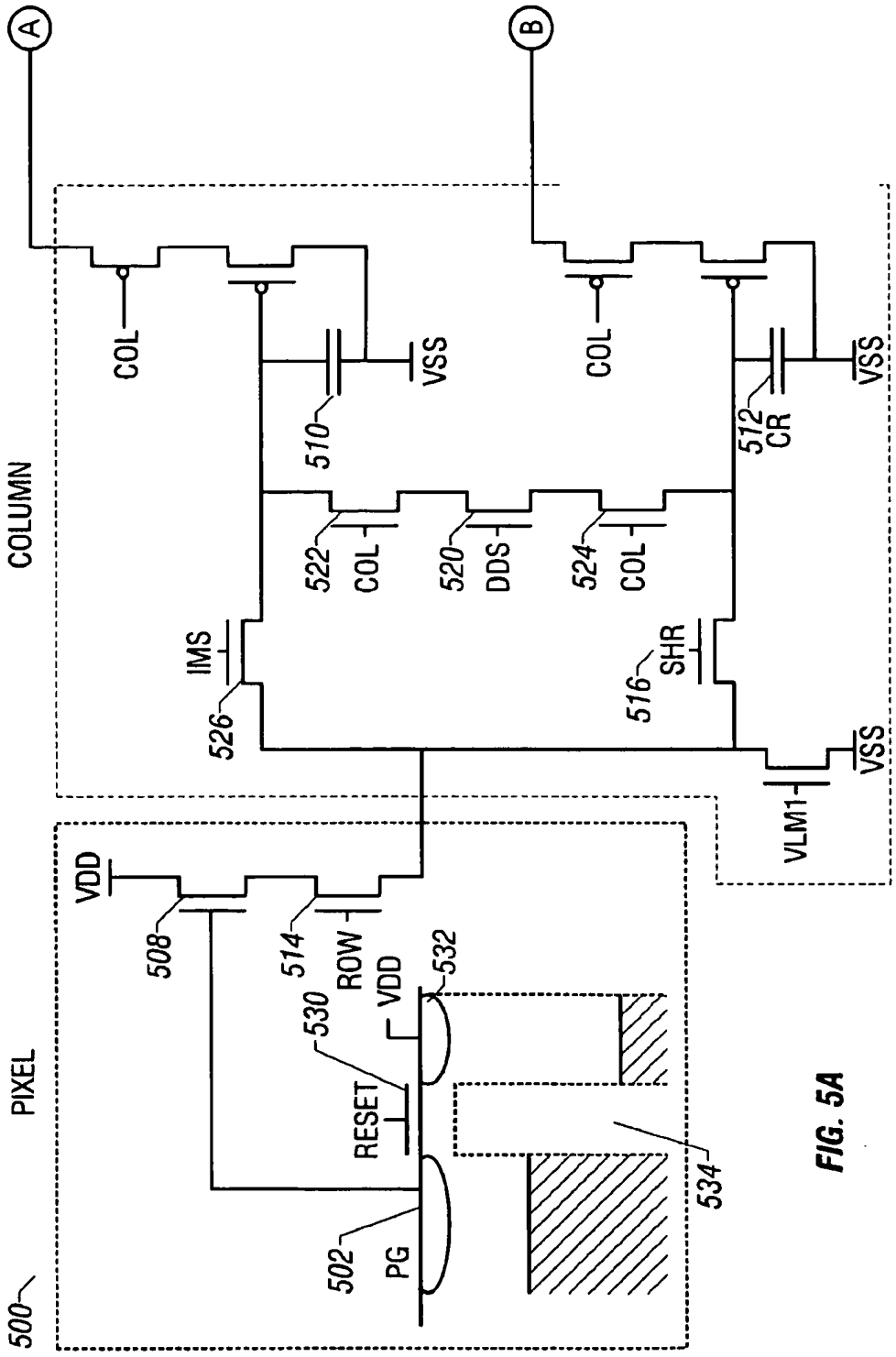

A
B
COL
VSS
510
512
CR
COLUMN
522
520
DDS
524
IMS
526
SHR
516
VLM1
VDD
508
514
ROW
532
530
RESET
534
PIXEL
502
PG
500

FIG. 5A

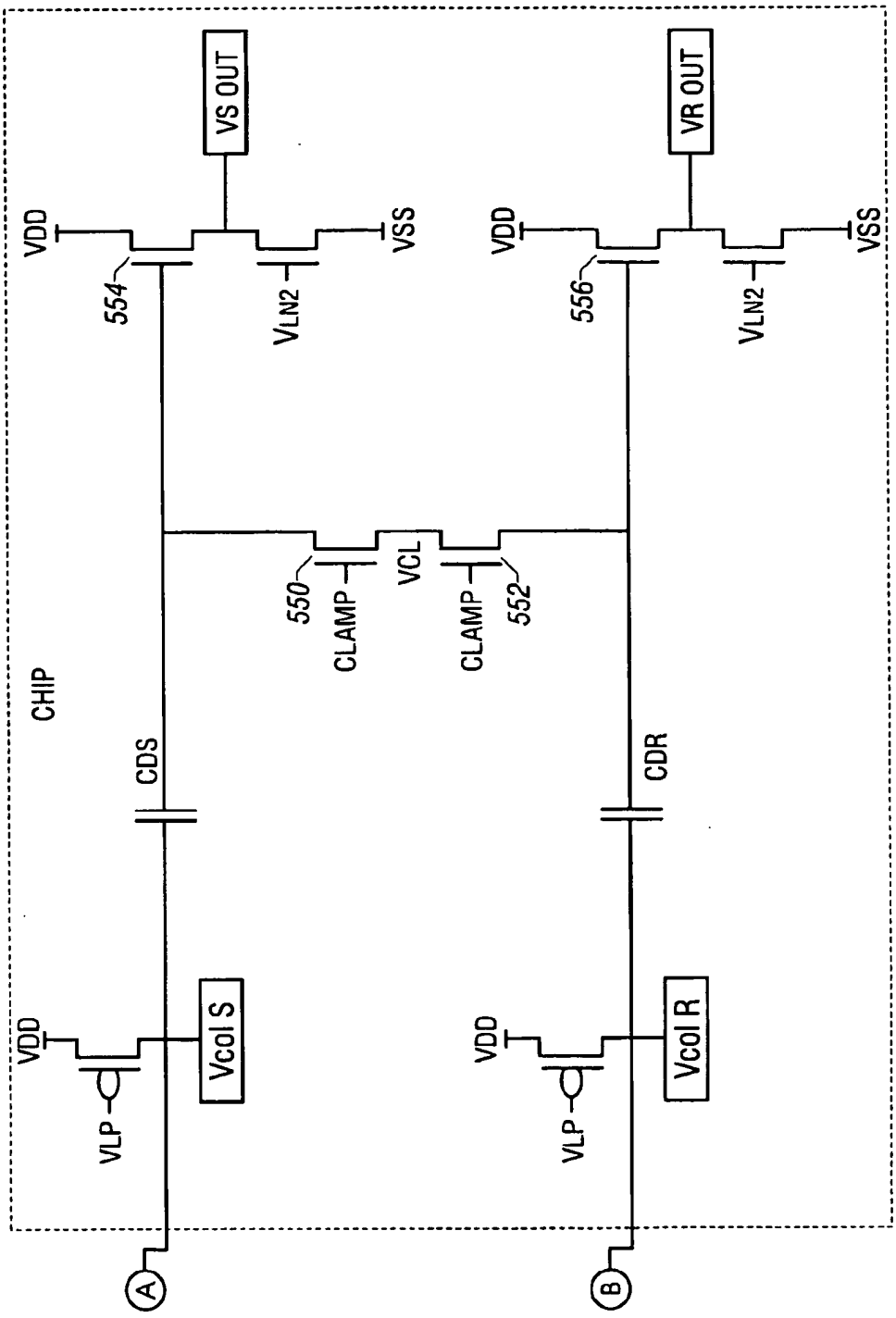

VS OUT
VR OUT
VDD
VSS
554
556
VLN2
550
552
CLAMP
VCL
CHIP
CDS
CDR
VLP
Vcol S
Vcol R
A
B

FIG. 5B

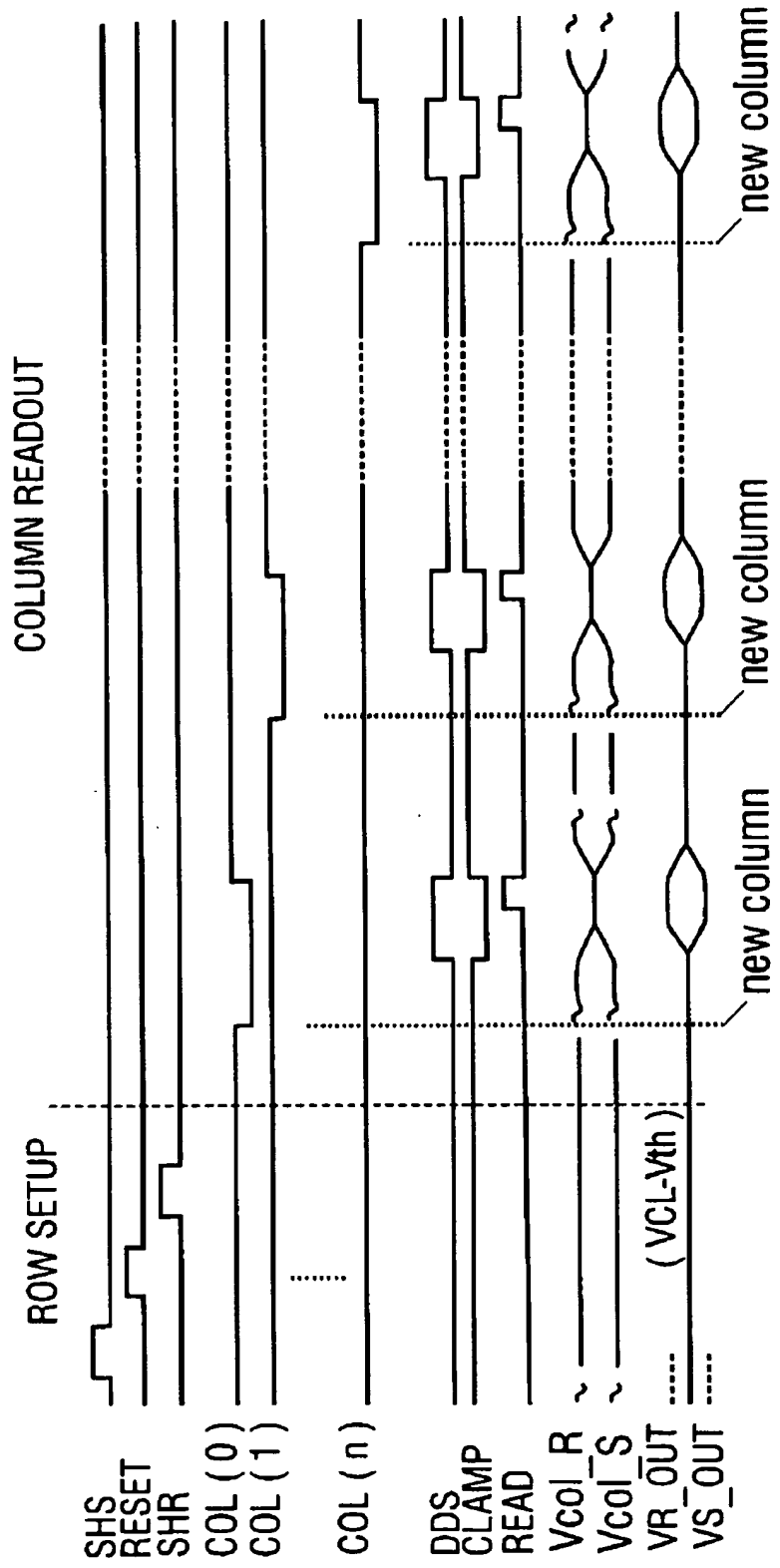

ROW SETUP
COLUMN READOUT
SHS
RESET
SHR
COL (0)
COL (1)
COL (n)
DDS
CLAMP
READ
Vcol_R
Vcol_S
VR_OUT
VS_OUT
(VCL-Vth))
new column
new column
new column

FIG. 6

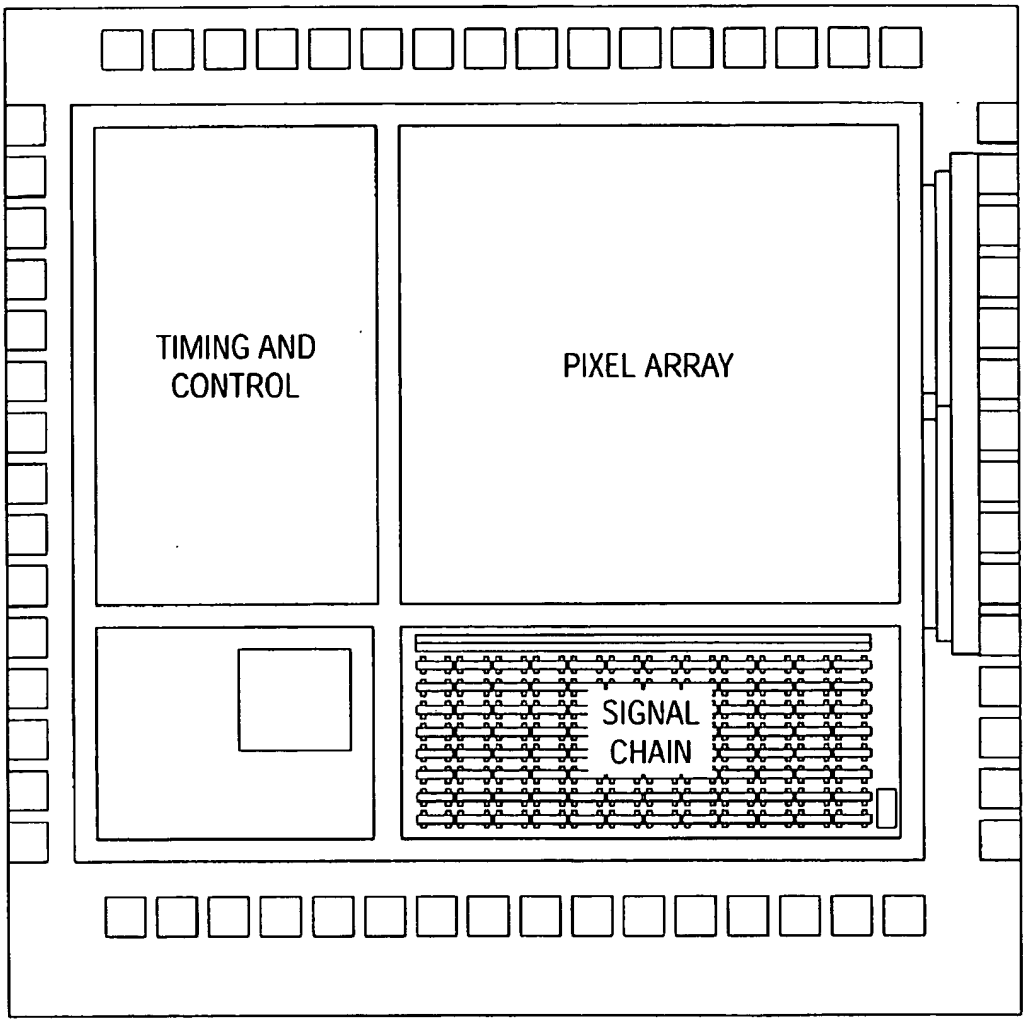


FIG. 7

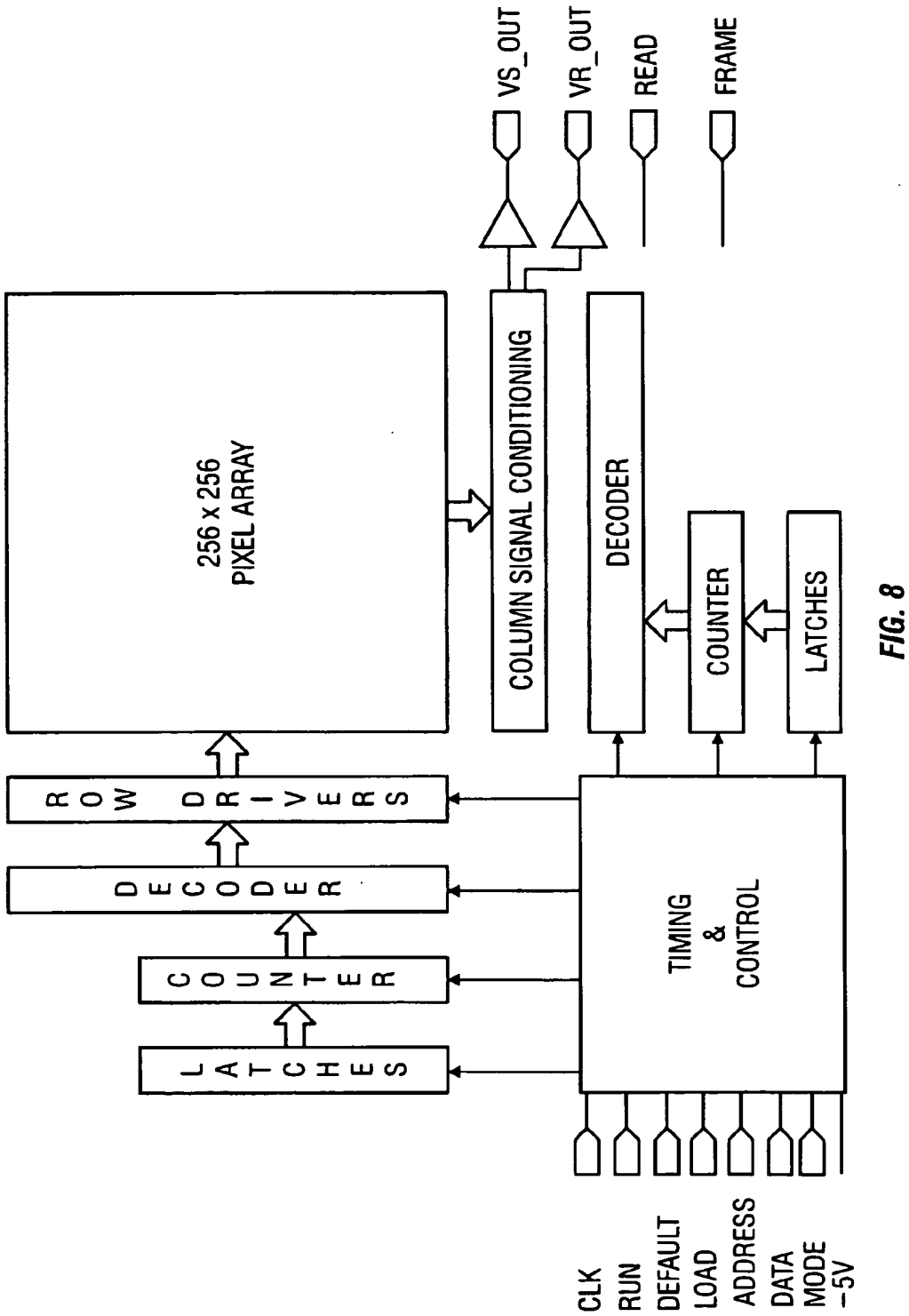
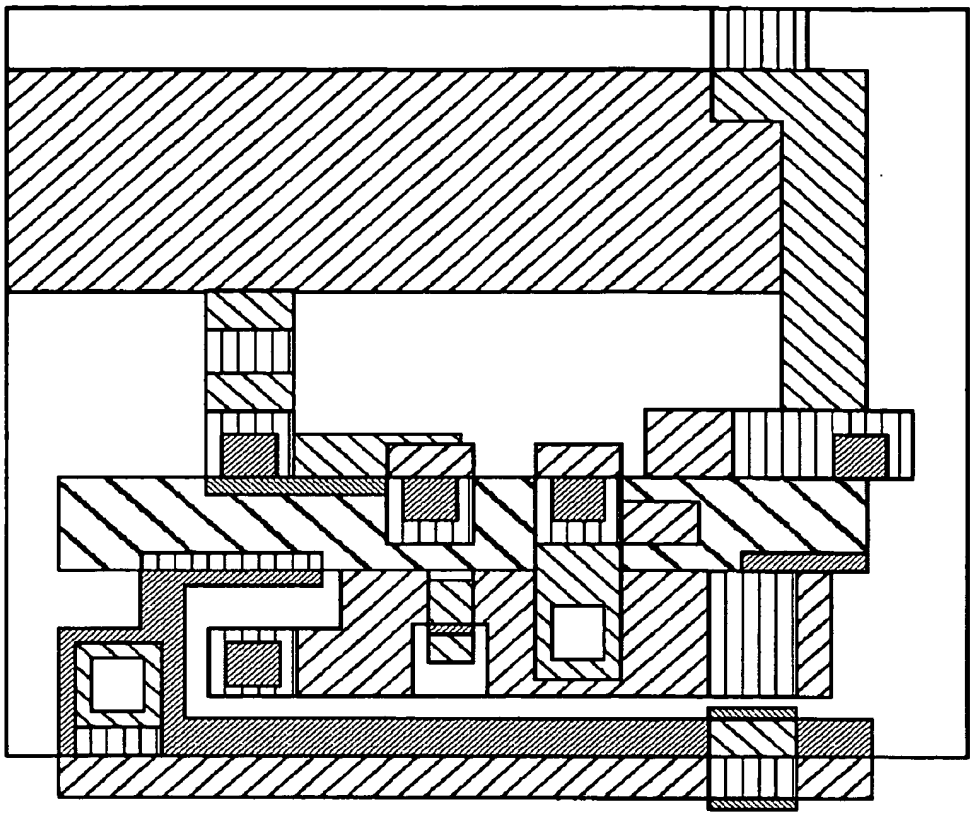

VS_OUT
VR_OUT
READ
FRAME
256 x 256
PIXEL ARRAY
COLUMN SIGNAL CONDITIONING
DECODER
COUNTER
LATCHES
ROW DRIVERS
DECODER
COUNTER
LATCHES
TIMING
&
CONTROL
CLK
RUN
DEFAULT
LOAD
ADDRESS
DATA
MODE
-5V

FIG. 8



Array Size	256 x 256
Pixel Size	20.4 μm
Technology	1.2 μm n-well CMOS (HP)
Maximum Clock Rate	10 MHz
Minimum Clock Rate	none
Maximum Pixel Rate	2.5 MHz
Maximum Integration Delay	16 x 10^9 clock periods or 1600 secs at 10 MHz

FIG. 8

SINGLE SUBSTRATE CAMERA DEVICE WITH CMOS IMAGE SENSOR

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. application Ser. No. 09/120,856, filed Jul. 21, 1998, which is a continuation of U.S. application Ser. No. 08/188,032, filed Jan. 28, 1994, and a continuation of U.S. application Ser. No. 08/789,608, filed Jan. 24, 1997, and claims priority to U.S. provisional application serial No. 60/010,678, filed Jan. 26, 1996. The disclosure of the prior applications is considered part of (and is incorporated by reference in) the disclosure of this application.

ORIGIN

[0002] The invention described herein was made in performance of work under NASA contract and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the contractor has elected to retain title.

FIELD OF THE INVENTION

[0003] The present invention relates to a single chip imaging sensor.

BACKGROUND AND SUMMARY OF THE INVENTION

[0004] Imaging technology is the science of converting an image to a signal indicative thereof. Imaging systems have broad applications in many fields, including commercial, consumer, industrial, medical, defense and scientific markets.

[0005] The original image sensors included an array of photosensitive elements in series with switching elements. Each photosensitive element received an image of a portion of the scene being imaged. That portion is called a picture element or pixel. The image obtaining elements produce an electrical signal indicative of the image plus a noise component. Various techniques have been used in the art to minimize the noise, to thereby produce an output signal that closely follows the image.

[0006] Size minimization is also important. The development of the solid state charge coupled device ("CCD") in the early 1970's led to more compact image systems. CCDs use a process of repeated lateral transfer of charge in an MOS electrode-based analog shift register. Photo-generated signal electrons are read after they are shifted into appropriate positions. However, the shifting process requires high fidelity and low loss. A specialized semiconductor fabrication process was used to obtain these characteristics.

[0007] CCDs are mostly capacitive devices and hence dissipate very little power. The major power dissipation in a CCD system is from the support electronics. One reason for this problem is because of the realities of forming a CCD system.

[0008] The specialized semiconductor fabrication process alluded to above is not generally CMOS compatible. Hence, the support circuitry for such a CCD has been formed using control electronics which were not generally CMOS compatible. The control electronics have dissipated an inordinate percentage of the power in such imaging devices. For example, CCD-based camcorder imaging systems typically operate for an hour on an 1800 mA-hr 6 V NiCad rechargeable battery, corresponding to 10.8 W of power consumption. Approximately 8 watts of this is dissipated in the imaging system. The rest is used by the tape recording system, display, and autofocus servos.

[0009] Space-based imaging systems often have similar problems. The space based systems operate at lower pixel rates, but with a lower degree of integration, and typically dissipate 20 watts or more.

[0010] The CCD has many characteristics which cause it to act like a chip-sized MOS capacitor. The large capacitance of the MOS device, for example, requires large clock swings, Δv, of the order of 5-15 V to achieve high charge transfer efficiency. The clock drive electronics dissipation is proportional to $C\Delta V^2 f$, and hence becomes large. In addition, the need for various CCD clocking voltages (e.g. 7 or more different voltage levels) leads to numerous power supplies with their attendant inefficiencies in conversion.

[0011] Signal chain electronics that perform correlated double sampling ("CDS") for noise reduction and amplification, and especially analog to digital converters (ADC), also dissipate significant power.

[0012] The inventors also noted other inefficiencies in imaging systems. These inefficiencies included fill factor inefficiencies, fixed pattern noise, clock pick up, temporal noise and large pixel size.

[0013] Active pixel sensors, such as described in U.S. Pat. No. 5,471,515, the disclosure of which is incorporated by reference herein, use special techniques to integrate both the photodetector and the readout amplifier into the pixel area or adjacent the pixel area. This allows the signal indicative of the pixel to be read out directly. These techniques have enabled use of a logic family whose fabrication processes are compatible with CMOS. This has enabled the controlling circuitry to be made from CMOS or some other low power-dissipating logic family.

[0014] The inventors of the present invention have recognized techniques and special efficiencies that are obtained by specialized support electronics that are integrated onto the same substrate as the photosensitive element. Aspects of the present invention include integration, timing, control electronics, signal chain electronics, A/D conversion, and other important control systems integrated on the same substrate as the photosensitive element.

[0015] It is hence an object of the present invention to provide for the integration of an entire imaging system on a chip.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] **FIG. 1** shows a basic block diagram of a CMOS active pixel circuit;

[0017] **FIG. 2** shows a graph of typical APS quantum efficiency;

[0018] **FIG. 3** shows the block diagram of the overall chip including drivers and controlling structures;

[0019] **FIGS. 4A and 4B** show the timing diagrams for photogate operation and photodiode operation, respectively;

[0020] FIG. 5 shows a schematic of the active pixel sensor unit cell and readout circuitry;

[0021] FIG. 6 shows a timing diagram for setup and readout;

[0022] FIG. 7 shows a drawing of an actual layout of the pixel and control circuitry;

[0023] FIG. 8 shows a block diagram of a CMOS APS chip; and

[0024] FIG. 9 shows an exemplary pixel layout.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] An active pixel sensor is herewith described with reference to FIGS. 1-4.

[0026] A block diagram of a CMOS active pixel circuit is shown in FIG. 1. The device has a pixel circuit 150, and a column circuit 155.

[0027] Incident photons pass through the photogate ("PG") 100 in the pixel circuit 150 and generate electrons which are integrated and stored under PG 100. A number of the pixel circuits are arranged in each row of the circuit. One of the rows is selected for readout by enabling the row selection transistor 102 ("RS").

[0028] In the preferred embodiment, the floating diffusion output node 104 ("FD") is first reset by pulsing reset transistor ("RST") 106. The resultant voltage on FD 104 is read out from the pixel circuitry onto the column bus 112 using the source follower 110 within the pixel. The voltage on the column bus 112 is sampled onto a first holding capacitor 114 by pulsing transistor SHR 116. This initial charge is used as the baseline.

[0029] The signal charge is then transferred to FD 104 by pulsing PG 100 low. The voltage on FD 104 drops in proportion to the number of photoelectrons and the capacitance of FD. The new voltage on the column bus 112 is sampled onto a second capacitor 118 by pulsing SHR 120. The difference between the voltages on first capacitor 114 and second capacitor 118 is, therefore, indicative of the number of photoelectrons that were allowed to enter the floating diffusion.

[0030] The capacitors 114, 118 are preferably 1-4 pf capacitors.

[0031] All pixels on a selected row are processed simultaneously and sampled onto capacitor at the bottom of their respective columns. The column-parallel sampling process typically takes 1-10 μsec, and preferably occurs during the so-called horizontal blanking interval of a video image.

[0032] Each column is successively selected for read-out by turning on column selection p-channel transistors ("CS") 130. The p-channel source-followers 122, 124 in the column respectively drive the signal (SIG) and horizontal reset (RST) bus lines. These lines are loaded by p-channel load transistors which can be sent directly to a pad for off-chip drive, or can be buffered.

[0033] Noise in the sensor is preferably suppressed by the above-described correlated double sampling ("CDS=38) between the pixel output just after reset, before and after signal charge transfer to FD as described above. The CDS suppresses kTC noise from pixel reset, suppresses 1/f noise from the in-pixel source follower, and suppresses fixed pattern noise (FPN) originating from pixel-to-pixel variation in source follower threshold voltage.

[0034] The inventors found, however, that kTC noise may be reintroduced by sampling the signal onto the capacitors 114, 118 at the bottom of the column. Typical output noise measured in CMOS APS arrays is of the order of 140-170 μV/e-, corresponding to noise of the order of 13-25 electrons r.m.s. This is similar to noise obtained in most commercial CCDs, through scientific CCDs have been reported with read noise in the 3-5 electrons rms.

[0035] Typical biasing for each column's source-follower is 10 μA. This permits charging of the sampling capacitors in the allotted time. The source-followers can then be turned off by cutting the voltage on each load transistor.

[0036] The sampling average power dissipation P_s corresponds to :

$$P_s = n\,I\,V\,d$$

[0037] where n is number of columns, I is the load transistor bias, V is the supply voltage, and d is the duty cycle. Using n=512, I=μA, V=5V and d=10%, a value for Ps of 2.5 mW is obtained.

[0038] A load current of 1 mA or more is needed to drive the horizontal bus lines at the video scan rate. The power, dissipated is typically 5 mW.

[0039] Quantum efficiency measured in this CMOS APS array is similar to that for interline CCDs. A typical response curve is shown in FIG. 2. The inventors noticed from this that the quantum efficiency reflects significant responsivity in the "dead" part of the pixel; the part containing the readout circuitry rather than the photogate collector. The responsiveness was measured by intra-pixel laser spot scanning.

[0040] The inventors postulate the following reason. The transistor gate and channel absorb photons with short absorption lengths (i.e. blue/green). However, longer wavelength photons penetrate through these regions. The subsequently-generated carriers diffuse laterally and are subsequently collected by the photogate.

[0041] Thus, despite a fill factor of 25%-30%, the CMOS APS achieves quantum efficiencies that peak between 30%-35% in the red and near infrared. Microlenses are preferably added to refract photoelectrons from the dead part to a live part and hence improve quantum efficiency.

[0042] An important feature of the system described herein is the integration of on-chip timing and control circuits within the same substrate that houses the pixel array and the signal chain electronics. A block diagram of the chip architecture is shown in FIG. 3.

[0043] The analog outputs VS_out (signal) and VR_out (reset) are as described above. The digital outputs include FRAME and READ. Most of the inputs to the chip are asynchronous digital signals, as described herein.

[0044] The chip includes a pixel array 300, which is driven by on-chip electronics. Timing and control circuit 302 drives row electronics 310, and column electronics 320.

[0045] The control circuits can command read-out of any area of interest within the array. Row decoder **312** controls row drivers **314** which can select a certain row for readout. A specific row is selected by entry of a row value **316** which is output from timing and control **302**. Row value **316** is stored in latch **318** which drives counter **319**. Counter **319** can allow selection of subsequent rows that follow the current row. Similarly, columns can be selected and accessed by latches **322**, counter **324**, decoder **326** and column signal conditioning **328**.

[0046] Each of the decoder counters can be preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus **330**. Therefore, as described above, selection of a row commands pixels in that row to be transferred to the appropriate row decoding elements, e.g., capacitors. Preferably there is one capacitor associated with each column. This provides for the sequential readout of rows using the column. The capacitors are preferably included within the column signal conditioner **328**. Column decoders **326** also allow selection of only a certain column to be read. There are two parts of each column selection: where to start reading, and where to stop reading. Preferably the operation is carried out using counters and registers. A binary up-counter within the decoder **326** is preset to the start value. A preset number of rows is used by loading the 2's compliment. The up counter then counts up until an overflow.

[0047] An alternate loading command is provided using the DEFAULT LOAD input line **332**. Activation of this line forces all counters to a readout window of 128×128.

[0048] A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus **330**. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. The counter can hence provide vary large integration delays. The input clock can be any frequency up to about 10 MHZ. The pixel readout rate is tied to one-fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. The integration time is therefore equal to the delay time and the readout time for a 2.5 MHZ clock. The maximum delay time is $2^{32}/2.5$ MHZ, or around 28 minutes. These values therefore easily allow obtaining a 30 Hz frame.

[0049] The timing and control circuit controls the phase generation to generate the sequences for accessing the rows. The sequences must occur in a specified order. However, different sequences are used for different modes of operation. The system is selectable between the photodiode mode of operation and the photogate mode of operation. The timing diagrams for the two gates are respectively shown in **FIGS. 4***a* and **4***b*. **FIG. 4***a* shows an operation to operate in the photogate mode and **FIG. 4***b* shows operating in the photodiode mode. These different timing diagrams show that different column operations are possible. Conceptually this is done as follows. Column fixed pattern noise is based on differences in source follower thresholds between the different transistors. For example, if the base bias on a transistor is V1, the output is V1 plus the threshold.

[0050] The column signal conditioning circuitry contains a double-delta sampling fixed pattern noise ("FPN") suppression stage that reduces FPN to below 0.2% sat with a random distribution. Since the APS is formed of a logic family that is compatible with CMOS, e.g., NMOS, the circuitry can be formed of CMOS. This allows power dissipation in the timing and control digital circuitry to be minimized and to scale with clock rate.

[0051] An active pixel sensor includes both a photodetector and the readout amplifier integrated within the same substrate as the light collecting device, e.g., the photodiode. The readout amplifier is preferably within and/or associated with a pixel.

[0052] A first embodiment of the present invention is a 128 ×128 CMOS photodiode type active pixel sensor that includes on chip timing, control and signal train electronics. A more detailed drawing of the chip is shown in **FIG. 5**. Asynchronous digital signals are converted by this chip to VS and VR analog outputs which are used to run the chip.

[0053] Pixel portion **500** includes a photodiode **502** which stores incident photons under photogate **504**. The photons are integrated as electrons within the photogate well. The output is buffered by follower **508**.

[0054] The rows are arranged into an array. A particular row is selected by the row transistor **514**. This allows the information from within the selected pixel **500** to be passed to the column decoder circuitry. Reset transistor **530** is connected to a sink **532**. Reset transistor is biased to a low potential level to allow all charge to bleed to sink **532**, and hence hold the stored charge in reset. The system is removed from reset by biasing the gate to a level as shown. This level is less than a highest possible potential to thereby allow charge which accumulates above that level to pass to sink **532**. Hence, the charge cannot overflow in an undesired way. This suppresses the blooming effect.

[0055] The depicted photogate system is driven according to the readout sequence shown in **FIG. 6**. A row is selected by activating row selecting transistor **514**. The cycle begins by sampling the signal present on each column pixel in that row. Sampling is initiated by biasing transistor **526** to place the signal from each column pixel in the row onto the holding capacitor **510**.

[0056] After the current pixel value has been transferred to the capacitor **510**, the pixel in the row is reset by biasing reset transistor to a low level, to photodiode **502** to the preset voltage sink **532**.

[0057] Correlated double sampling is effected by sampling the reset value, as a reset level, onto the holding capacitor **512**. This is done by activating the reset transistor **516**.

[0058] The voltage value of the reset branch of the column circuit is given by

$$Vcol\_R \propto \beta\{\alpha[V_{pdr}-V_{tpix}]-V_{tcolr}\}$$

[0059] Where α is the gain of the pixel source follower **508**, β is the gain of the column source follower **526**, and V_{pdr} is the voltage on the photodiode after reset, V_{tpix} is the threshold voltage of the pixel source follower and channel transistor, and V_{tcolr} is the threshold voltage of the column source follower p-channel transistor.

[0060] Using similar reasoning, the output voltage of the signal branch of the column circuit is

$$Vcol\_S \propto \beta\{\alpha[V_{pds}-V_{tpix}]-V_{tcols}\}$$

[0061] where V_{pds} is the voltage on the photodiode with the signal charge present and V_{tcols} is the threshold voltage of the column source-follower p-channel transistor.

[0062] The inventors have found experimentally that the peak-to-peak variation $V_{tcolr-Vtcols}$ is typically between 10 and 20 millivolts. This, however, is a source of column to column fixed pattern noise. The inventors herein suggest a double delta sampling technique to eliminate this column to column noise. The present approach represents an improved version of the previously-described double delta sampling circuitry. The operation proceeds as follows. A column is first selected. After a settling time equivalent to half of the column selection period, a special double delta sampling technique is performed to remove the column fixed pattern noise. Therefore, the varying thresholds on the different transistors cause varying outputs. According to this aspect, the threshold outputs of these transistors are equalized using a capacitor to equalize the charge. The capacitor is applied with the charge before and after the voltage change. Therefore, the output of the capacitor represents the difference between before and after, and the fixed pattern noise component drops out of the equation.

[0063] This system uses a DDS switch **520** and first and second column select switches **522, 524** to short across the respective capacitors. All three switches are turned on to short across the two sample and hold capacitors **510**. This clamp operation is shown in line **8** of **FIG. 6**.

[0064] Prior to the DDS operation, the reset and signal column components, Vcol_R and Vcol_S include their signal values plus a source follower voltage threshold component from the appropriate source follower. The object of the special following circuit of the present invention is to remove that source follower threshold component. The operation proceeds as follows. Prior to the beginning of some operation, the capacitors are precharged through clamp transistors to a clamp voltage V_{cl}. This is maintained by turning on clamp transistors **550** and **552** to connect the appropriate capacitors to the voltage V_{cl}. The clamp operation is shown on line **8** of **FIG. 6**. Immediately after the clamp is released, the DDS transistors **520, 522** and **524** are turned on. This has the effect of shorting across the capacitors **510** and **512**. When the transistors are shorted, the voltage that is applied to the output drivers **554, 556** includes only the voltage threshold component. The differential amplification of the voltage render the output voltage free of the voltage threshold component. Mathematically, prior to clamp being deactivated the output signals are:

$$VR\_OUT=Y\ (V_{cl}-V_{tr})$$

and $$VS\_OUT=Y\ (V_{cl}-V_{ts})$$

[0065] where Y is the gain of the third stage source-follower, V_{cl} is the clamp voltage, and V_{tr} and V_{ts} are the threshold voltages of the third stage source-follower n-channel transistors, reset and signal branch respectively. Deactivation of the clamp circuit and simultaneous activation of the DDS switch causes several changes. The voltages in the two column branch sampling circuits equalize becoming:

$$V_{cs}=V_{cr}=\alpha[V_{pdr}-V_{tptx}+V_{pds}-V_{tptx}]/2$$

[0066] This in turn causes a change in Vcol_S and Vcol_R to:

$$Vcol\_R'=\beta\{\alpha[V_{pdr}-V_{tptx}+V_{pds}-V_{tptx}]/2-V_{tcolr}\}$$

and $$Vcol\_S'=\beta\{\alpha[V_{pdr}-V_{tptx}+V_{pds}-V_{tptx}]/2-V_{tcols}\}$$

[0067] Consequently, the voltage outputs change to:

$$VR\_OUT=Y\ (V_{cl}-Vcol\_R'-Vcol\_R-V_{tr})$$

and $$VS\_OUT=Y\ (V_{cl}-Vcol\_S'-Vcol\_S-V_{ts})$$

[0068] We note

$$Vcol\_S'-Vcol\_S=\beta\{\alpha[V_{pds}-V_{pdr}]/2\}$$

and $$Vcol\_R'-Vcol\_R=\beta\{\alpha[V_{pdr}-V_{pds}]/2\}$$

[0069] When the outputs are differentially amplified off-chip, the common clamp voltage Vcl is removed, leaving only the difference between signal and reset. The net differential output voltage is given by:

$$VR\_OUT-VS\_OUT=\alpha\beta Y\ (V_{pdr}-V_{pds}=V_{const})$$

[0070] **FIG. 7** shows the layout of the pixel for 128x128 array size device. This system formed a 19.2 micron pixel size using 1.2 μm n-well CMOS. The maximum clock rate is 10 MHZ, the maximum pixel rate is 2.5 MHZ and maximum integration delay is 1.6x109 clock periods.

[0071] A second embodiment uses similar design techniques to produce a 256x256 array size. This embodiment also uses a pixel with a photogate imaging element along with four transistors to perform the functions of readout, selection, and reset. Readout is preferably achieved using a column parallel architecture which is multiplexed one row at a time and then one column at a time through an on-chip amplifier/buffer. An important part of this embodiment, like the first embodiment, is the use of a chip common logic elements to control row and address decoders and delay counters.

[0072] This embodiment allows use in three modes of operation: Photogate mode, photodiode mode and differencing mode. The photogate mode is the standard mode for this chip. The photodiode mode alters the readout timing to be similar to that for photodiode operation. The differencing mode alters the readout timing in such a way that the value of each pixel output is the difference between the current frame and the previous frame. The chip inputs that are required are a single +5 V power supply, start command, and parallel data load commands for defining integration time and windowing parameters. The output has two differential analog channels.

[0073] The second embodiment uses the block diagram of the chip architecture shown in **FIG. 8**. The analog outputs of VS_OUT (signal) and VR_OUT (reset), and digital outputs of FRAME and READ. The inputs to the chip are asynchronous digital signals. The chip includes addressing circuitry allowing readout of any area of interest within the 256x256 array. The decoder includes counters that are preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus. An alternate loading command is provided using the DEFAULT input line. Activation of this line forces all counters to a readout window of 256x256.

[0074] A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each

frame from the latch. This counter allows forming very large integration delays. The input clock can be any frequency up to about 10-MHZ. The pixel readout rate is tied to one fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. A 30 HZ frame rate can be achieved without difficulty.

[0075] The chip is idle when the RUN command is deactivated. This is the recommended time for setting the operating parameters. However, these parameters can be set at any time because of the asynchronous nature of operation. When RUN is activated, the chip begins continuous readout of frames based on the parameters loaded in the control registers. When RUN is deactivated, the frame in progress runs to completion and then stops.

[0076] The 256×256 CMOS APS uses a system having a similar block diagram to those described previously. The pixel unit cell has a photogate (PG), a source-follower input transistor, a row selection transistor and a reset transistor. A load transistor VLN and two output branches to store the reset and signal levels are located at the bottom of each column of pixels. Each branch has a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a source-follower with a column-selection switch (COL). The reset and signal levels are read out differentially, allowing correlated double sampling to suppress 1/f noise and fixed pattern noise (not kTC noise) from the pixel.

[0077] A double delta sampling (DDS) circuit shorts the sampled signals during the readout cycle reducing column fixed pattern noise. These readout circuits are common to an entire column of pixels. The load transistors of the second set of source followers (VLP) and the subsequent clamp circuits and output source followers are common to the entire array. After a row has been selected, each pixel is reset (RESET) and the reset value is sampled (SHR) onto the holding capacitor CR. Next, the charge under each photogate in the row is transferred to the floating diffusion (FD). This is followed by sampling this level (SHS) onto holding capacitor CS. These signals are then placed on the output data bus by the column select circuitry. In the Photodiode mode this process, is reversed; first the charge under the photogate is read out and then the reset level is sampled. This non-correlated double sampling mode would be primarily used with a photodiode, i.e., non active pixel sensor, pixel.

[0078] In the differencing mode, the capacitors CS and CR are used to store the signal from the previous frame and the current frame. This is achieved by altering the timing in the following way: Rather than starting with a reset operation, the signal on the floating diffusion is read out to one of the sample and hold capacitors. This represents the previous pixel value. The reset is then performed followed by a normal read operation. This value is then stored on the other sample and hold capacitor. The difference between these two signals is now the frame to frame difference.

[0079] A simplified expression for the output of the reset branch of the column circuit is given by:

$$Vcol\_R=\beta\{\alpha[Vr-V_{tpix}]-V_{tcolr}\}$$

[0080] where α is the gain of the pixel source-follower, β is the gain of the column source-follower, Vr is the voltage on the floating diffusion after reset, V_{tpix} is the threshold voltage of the pixel source-follower n-channel transistor, and V_{tcolr} is the threshold voltage of the column source-follower p-channel transistor. Similarly, the output voltage of the signal branch of the column circuit is given by:

$$Vcol\_S=\beta\{\alpha[V_S-V_{tpix}]-V_{tcols}\}$$

[0081] where V_s is the voltage on the floating diffusion with the signal charge present and V_{tcols} is the threshold voltage of the column source-follower p-channel transistor. Experimentally, the peak to peak variation in $V_{tcolr}-V_{tcols}$ is typically 10-20 mV. It is desirable to remove this source of column-to-column fixed pattern noise FPN. JPL has previously developed a double delta sampling (DDS) technique to eliminate the column-to-column FPN. This approach represented an improved version of the DDS circuitry.

[0082] Sequential readout of each column is as follows. First a column is selected. After a settling time equivalent to one-half the column selection period, the DDS is performed to remove column fixed pattern noise. In this operation, a DDS switch and two column selection switches on either side are used to short the two sample and hold capacitors CS and CR. Prior to the DDS operation the reset and signal outputs (Vcol_R and VCOL_S) contain their respective signal values plus a source follower voltage threshold component. The DDS switch is activated immediately after CLAMP is turned off. The result is a difference voltage coupled to the output drivers (VR_OUT and VS_OUT) that is free of the voltage threshold component.

[0083] This chip uses a similar pixel cell to that shown in **FIG. 5. FIG. 9** shows the layout of the pixel cell. PG and RESET are routed horizontally in polysilicon while the pixel output is routed vertically in metal1. Metal2 was routed within the pixel for row selection. Metal2 was also used as a light shield and covers most of the active area outside of the pixel array. The designed fill factor of the pixel is approximately 21%.

[0084] According to another feature, a logo can be formed on the acquired image by using a light blocking metal light shield. The light shield is formed to cover certain pixels in the shape of the logo to be applied. This blocks out those underlying pixels in the array, thereby forming a logo in the shape of the blocked pixels.

[0085] The output saturation level of the sensor is 800 mv when operated from a 5 V supply. Saturation is determined by the difference between the reset level on the floating diffusion node (e.g. 3 V) and the minimum voltage allowed on the pixel source follower gate (e.g. threshold voltage of approx. 0.8 volts). This corresponds to a full well of approximately 75,000 electrons. This can be increased by operating at a larger supply voltage, gaining about 47,000 e– per supply volt.

[0086] Dark current was measured at less than 500 pA/cm^2.

[0087] Conversion gain (μV/e–) was obtained per pixel by plotting the variance in pixel output as a function of mean signal for flat field exposure. The fixed pattern noise arising from dispersion in conversion gain was under 1%—similar to the value found in CCDs and consistent with the well-controlled gain of a source-follower buffer.

[0088] The quantum efficiency of the detector was measured using a CVI ¼ m monochromator and a tungsten/halogen light source, calibrated using a photodiode traceable to NIST standards.

What is claimed is:

1. A single chip camera device, comprising:

a substrate;

an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS and both integrated in said substrate;

said image acquisition portion including an array of active pixel type photoreceptors integrated in said substrate, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;

said control portion including a signal controlling device integrated in said substrate, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors.

2. A camera device as in claim 1 wherein said array of photoreceptors are controlled to output an entire row of said photoreceptors simultaneously.

3. A camera device as in claim 1, wherein said photoreceptors include photodiodes.

4. A camera device as in claim 1, wherein said photoreceptors include photogates.

5. A single chip camera device, comprising;

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors.

6. A camera device as in claim 5, wherein said signal controlling device includes a column-parallel read out device, which reads out a row of said photoreceptors at substantially the same time.

7. A camera device as in claim 5, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for read out.

8. A camera device as in claim 5, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

9. A camera device as in claim 8, wherein said readout amplifier is preferably within and/or associated with one element of the array.

10. A camera device as in claim 8, wherein said photoreceptors are photodiodes.

11. A camera device as in claim 8, wherein said photoreceptors are photogates.

12. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion including an array of photoreceptors arranged in rows and columns;

a charge storage element, associated with each said column;

said control portion including a signal controlling device, controlling said photoreceptors to output their signals, and a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

said control portion including common logic elements to control all pixels on a selected row to sample said all pixels onto said charge storage elements substantially simultaneously.

13. A device as in claim 12, wherein said logic elements control said pixels to first sample a reset level of each said row, and then to sample a charged level of said charge storage elements to produce information indicating a correlated signal indicative of a difference therebetween.

14. A device as in claim 12, wherein said control portion includes a plurality of column selection p-channel transistors, respectively associated with each column, said transistors being turned on to sample a column.

15. A device as in claim 12, wherein there is one of said charge storage elements associated with each of said columns.

16. A device as in claim 12, wherein there are two of said charge storage elements associated with each of said columns.

17. A camera device as in claim 12, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

18. A camera device as in claim 17, wherein said readout amplifier is preferably within and/or associated with one element of the array.

19. A camera device as in claim 17, wherein said photoreceptors are photodiodes.

20. A camera device as in claim 17, wherein said photoreceptors are photogates.

* * * * *

United States Patent [19]

Berger et al.

[11] **Patent Number: 4,609,825**

[45] **Date of Patent: Sep. 2, 1986**

[54] **DEVICE FOR MODULATING THE SENSITIVITY OF A LINE-TRANSFER PHOTOSENSITIVE DEVICE**

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[73] Assignee: **Thomson-CSF, Paris, France**

[21] Appl. No.: **562,463**

[22] Filed: **Dec. 16, 1983**

[30] **Foreign Application Priority Data**

Dec. 23, 1982 [FR] France 82 21628

[51] **Int. Cl.**[4] **H01J 40/14; H04N 3/14**

[52] **U.S. Cl.** **250/578;** 358/213

[58] **Field of Search** ..... 250/211 J, 211 R, 578; 357/24 LR; 358/212, 213

[56] **References Cited**

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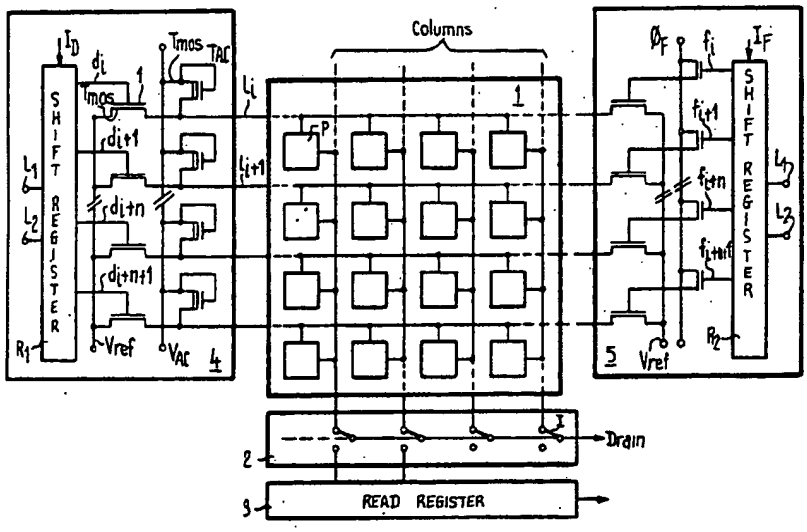
Assistant Examiner—Michael Messinger

Attorney, Agent, or Firm—Roland Plottel

[57] **ABSTRACT**

In order to modulate the sensitivity of a photosensitive device by modulating the integration time, a first reading of each line of a photosensitive zone of the device is followed by a second reading at an adjustable time interval. The charges resulting from the first reading operation are removed to the drain while the parasitic charges and the signal charges resulting from the second reading operation are transferred to the read register at the same time. Modulation of the time interval which elapses between two readings of one line is carried out by varying the time which elapses between the injection of one drive pulse into the two registers which control respectively the first reading and the second reading of the lines.

8 Claims, 3 Drawing Figures



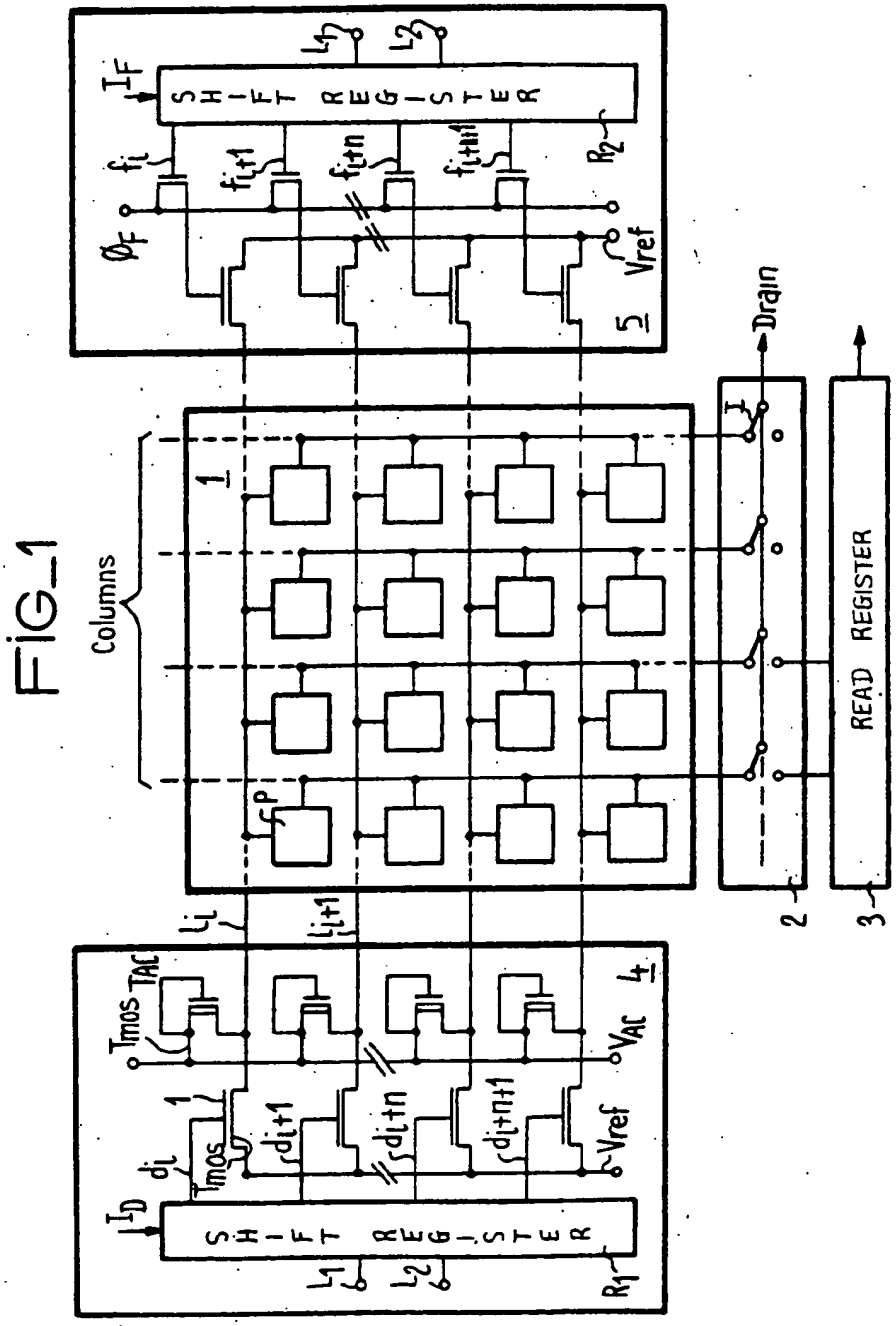

SHIFT REGISTER
Drain
READ REGISTER
Columns
SHIFT REGISTER
Vref
Vref

FIG_1

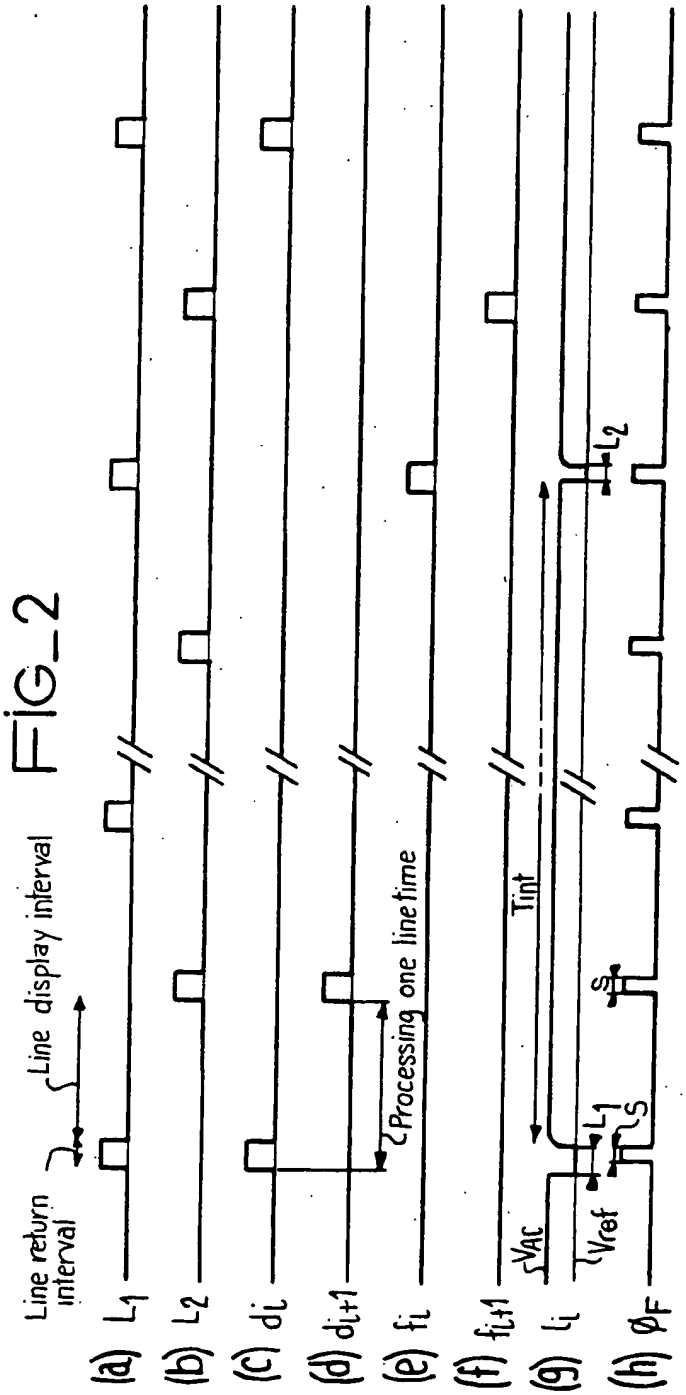

Line return interval
Line display interval
(a) L_1
(b) L_2
(c) d_i
(d) d_{i+1}
(e) f_i
(f) f_{i+1}
(g) l_i
(h) ϕ_F
Processing one line time
Tint
V_{AC}
V_{ref}
L_1
L_2
S

FIG_2

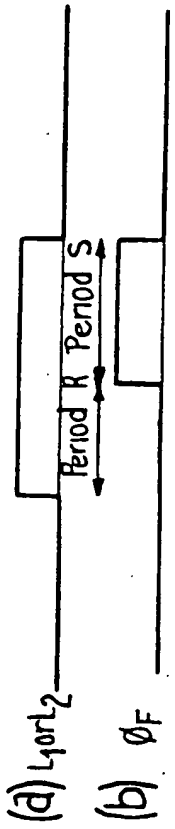

(d) L_1 or L_2
Period R Period S
(b) ϕ_F

FIG_3

DEVICE FOR MODULATING THE SENSITIVITY OF A LINE-TRANSFER PHOTOSENSITIVE DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a device for modulating the sensitivity of a line-transfer photosensitive device.

Photosensitive devices in which scanning is performed by line transfer are already known and have been described in particular in French patent Applications No. 80 09112 and No. 81 07672 filed in the name of Thomson-CSF.

2. Description of the Prior Art

It will be recalled in general terms that a device of this type has a photosensitive zone consisting of M lines each made up of N photosensitive points. The photosensitive points of the different lines are connected in parallel to a memory by means of conductive columns. The signal charges collected on a line of photosensitive points and transferred to the columns are caused by the memory to undergo a periodic transfer from the columns to a read register. In addition, the parasitic charges which are present in tne columns before the signal charges of one of the lines arrive on the columns are periodically transferred by the memory to an evacuation drain.

Known types of line-transfer photosensitive devices have a light sensitivity which is not variable. However, for the different applications of these devices such as cameras available to the general public or in the field of robotics and the like, it is an advantage to have the possibility of using the equivalent of a diaphragm or, in other words, of modulating the sensitivity of the device as a function of the incident light.

It is known to modulate the sensitivity of photosensitive devices in the solid state by varying their integration time.

Up to the present time, however, the basic design concept of line-transfer devices having a light sensitivity which can be varied by modulating the integration time has given rise to problems and the present invention provides the answer to these problems.

SUMMARY OF THE INVENTION

As hereinafter set forth in claim 1, this invention relates to a device for modulating the sensitivity of a line-transfer photosensitive device having a photosensitive zone made up of M lines of N photosensitive points. The photosensitive points of the different lines are connected in parallel by conductive columns to a memory which has the function of transferring to a read register the signal charges of one and the same line and of transferring to an evacuation drain the parasitic charges which are present in the columns prior to arrival of the signal charges. The distinctive feature of the modulating device lies in the fact that it comprises first and second means having the following functions:

the first means carry out a first reading of each line during the time interval which elapses when the charges derived from the columns are removed by the memory to the evacuation drain so that the charges resulting from the first reading operation are consequently removed to the drain at the same time as the parasitic charges;

after an adjustable time interval, the second means carry out a second reading of each line during the time interval which elapses when the charges derived from the columns are transferred by the memory into the read register so that the signal charges resulting from the second reading operation are consequently transferred to the read register.

The device in accordance with the invention offers a number of advantages. Of particular interest is the advantage arising from the availability of electronic modulation of sensitivity as compared with sensitivity modulations involving the use of mechanical control systems which actuate a diaphragm and are very cumbersome.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features of the invention will be more apparent upon consideration of the following description and accompanying drawings, wherein:

FIG. 1 is a schematic diagram showing one embodiment of the device in accordance with the invention;

FIGS. *2a* to *2h* and FIGS. *3a* and *3b* are waveform diagrams representing the drive signals employed in the device of FIG. 1.

In the different figures, the same references designate the same elements but the dimensions and proportions of the various elements have not been observed for the sake of enhanced clarity.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of one embodiment of the device in accordance with the invention.

In this figure, there is shown a photosensitive zone 1 constituted by a matrix of M lines each made up of N photosensitive points P. This zone receives the light image to be scanned and converts the image to electric charges known as signal charges Q_S. The photosensitive points of a given column are interconnected by one and the same conductive column. The conductive columns terminate in a memory 2. This memory comprises switching means which are represented schematically by switches I and conduct the charges which are present in the conductive columns either to an evacuation drain or to a read register 3. The memory therefore carries out periodic transfer to the read register of the signal charges Q_S which are collected on a line of photosensitive points and transferred to the columns. In addition, the parasitic charges which are present in the columns before the charge signals of one of the lines arrive in the columns and periodically transferred by the memory to an evacuation drain.

In the prior art, the photosensitive points of any one line are connected to each other as well as to an address register which makes it possible to select the matrix line which is to be read. Provision can be made for two address registers, one register being used for addressing the even-numbered lines and the other register being used for addressing the odd-numbered lines.

In the prior art, the integration time of the different lines is constant. The photosensitive points continuously integrate the charges created by the radiation to be scanned except during the few microseconds required in order to permit each line to deliver in turn the charges which it has integrated in the columns.

The invention makes it possible to obtain a modulation of sensitivity of the photosensitive device by varying the integration time of the photosensitive points.

The invention consists in performing in the case of each line a first reading operation and a second reading operation between which an adjustable time interval is allowed to elapse. The charges resulting from the first reading operation are removed to the drain while the parasitic charges and the signal charges resulting from the second reading operation are transferred at the same time to the read register.

The integration time of the different lines is constituted by the time interval which elapses between the first and the second reading operations. A variable integration time is obtained by varying this time interval.

As shown in FIG. 1, the device in accordance with the invention therefore comprises first means 4 whereby the first reading of each line takes place during the time taken by the memory to remove the charges from the columns to the drain. The device further comprises second means 5 whereby, after an adjustable time interval, the second reading of each line takes place during the time taken by the memory to transfer the charges from the columns into the read register.

In the embodiment of the invention shown in FIG. 1, the first and second means aforesaid comprise a shift register having M stages which addresses the M lines of the photosensitive zone by means of transistors.

A drive pulse is applied to the input of each register and transferred periodically from one stage of the register to the next. Modulation of the time interval which elapses between the first and the second reading operation is achieved by varying the elapsed time interval between injection of the drive pulse I_D and injection of the drive pulse I_F into each register R_1 and R_2.

The shift registers R_1 and R_2 of the means 4 and 5 are preferably shift registers formed by means of MOS transistors and controlled by two phases L_1 and L_2.

The device in accordance with the invention will now be described in detail in order to explain the operation of the embodiment shown in FIG. 1, reference being made to FIGS. 2*a* to 2*h* and to FIGS. 3*a* and 3*b* which represent the control signals of the device. It is postulated in the following description that the photosensitive points are constituted by MOS-phototransistors or by the association of MOS-phototransistors and photodiodes and are formed on a P-type semiconductor substrate.

In this embodiment, the shift registers R_1 and R_2 are controlled by the same addressing signals L_1 and L_2 which are represented in FIGS. 2*a* and 2*b*.

The signals L_1 and L_2 are at the high level during one line return interval out of two. It is recalled that photosensitive devices are usually required to be compatible with conventional television standards. In the case of the 625-line standard, an interval of approximately 52 μs is available for display of a line and an interval of 12 μs is available for the line return.

The drive pulse I_D and I_F which is applied to the input of each register R_1 and R_2 is present on one of the outputs of these registers during each line return interval.

FIGS. 2*c* and 2*d* and FIGS. 2*e* and 2*f* are representations of the signals obtained at the outputs d_i and d_{i+1} of the register R_1 and at the outputs f_i and f_{i+1} of the register R_2. These outputs address two consecutive lines l_i and l_{i+1} of the photosensitive zone.

The time interval which elapses between passages of the drive pulse from one stage of a register to the next is equal to the time taken for processing one line.

In the embodiment of FIG. 1, the stages of the register R_1 of the first means 4 are connected to a series of enhancement-mode MOS transistors designated by the reference TMOS-1. These transistors TMOS are connected on the one hand to one of the lines of the photosensitive zone and on the other hand to a bias voltage. When this bias voltage is applied to the gates of the MOS-phototransistors, it permits transfer of the charges stored by these points to the columns, that is to say the reading of one line. In FIG. 1, this voltage is the reference voltage Vref of the device. The gate of the transistors TMOS-1 is connected to one stage of the shift register R_1. The arrival of the drive pulse I_D on a stage initiates conduction of the transistor TMOS-1 which is associated with this stage and initiates reading of the corresponding line of the photosensitive zone which receives the bias voltage Vref.

The first means 4 of FIG. 1 comprise another series of depletion-mode MOS transistors designated by the reference TMOS-TAC. These transistors are mounted as emitter-followers between one line of the photosensitive zone and a bias voltage V_{AC} which permits integration of the charges when this voltage is applied to the MOS-phototransistors.

The departure of the drive pulse I_D from a stage has the effect of cutting-off the transistor TMOS-1 which is associated with this stage. At this instant, the corresponding transistor TMOS-TAC applies the voltage V_{AC} to the line which is addressed by said stage, thus bringing to an end the reading of charges of said line and marking the start of its integration period.

FIG. 2*g* represents the bias voltage received by the line l_i of the photosensitive zone. This voltage undergoes a transition from V_{AC} to Vref during the line return interval in which the drive pulse I_D is present on the output d_i of the register R_1.

It has been seen earlier that, in line-transfer photosensitive devices, there is a periodic recurrence of the two following sequences:

a first sequence corresponding to transfer to memory of the parasitic charges which are present in the columns, prior to arrival of the signal charges in the columns;

a second sequence corresponding to transfer to memory of the signal charges of one line which are present in the columns.

In the embodiment of FIG. 1, these two sequences take place during the line return interval. The line return interval is composed of two periods as shown in FIG. 3*a*, namely a period R during which the first sequence takes place followed by a period S during which the second sequence takes place.

The reading operation which is carried out on line l_i (as shown in FIG. 2*g*) whilst the drive pulse is present on the output d_i begins with the start of the line return interval during a period R. The charges transferred from line l_i to the columns are therefore removed to the memory and then to the drain. The end of the line return interval marks the end of the first reading L_1 of the line l_i and the beginning of the integration period Tint of this line.

The outputs of the register R_2 of the means 5 are connected to the gates of MOS transistors designated by the reference TMOS-F. The transistors TMOS-F are connected on the one hand to a clock signal ϕ_F shown in FIGS. 2*h* and 3*b* which changes to the high level during the period S of the line return interval and on the other hand to the gates of another series of MOS transistors designated by the reference TMOS-2.

A transistor TMOS-F is triggered into conduction when the drive pulse I_F arrives on the stage of the register to which said transistor is connected but remains in the conducting state only during the period S of the line return interval under the action of the signal ϕ_F

Each transistor TMOS-F drives the gate of a transistor TMOS-2 which is connected to a line of the photosensitive zone and to the bias voltage Vref which permits reading of the points of one line.

A transistor TMOS-F in the conducting state applies the bias voltage Vref to the corresponding line of the photosensitive zone via the transistor TMOS-2 and therefore initiates reading of said line.

In FIG. 2g, it is apparent that the second reading L_2 of the line l_i takes place during the period S of the line return interval while the pulse I_F is present on the output f_i. The beginning of this second reading operation marks the end of the integration period of the line l_i.

The second reading L_2 of the line l_i takes place during the period S of the line return interval, with the result that the charges transferred from the line l_i to the columns are sent to the read register 3 via the memory.

The integration time of the lines of the photosensitive zone is therefore varied by modulating the time interval which elapses between the arrival of a drive pulse on the outputs d_i and f_i of the two registers which address the same line l_i of the photosensitive zone.

During each line return interval, there is therefore carried out in the method according to the invention first of all the first reading L_1 of a line l_{i+n} for example, during the period R, and then the second reading L_2 of a line l_i for example, during the period S.

The invention makes it possible to vary the integration time to a considerable extent. The readings L_1 and L_2 of a line l_i can be performed during two consecutive line return intervals. In this case the integration period is 64 μs in the 625-line standard. The integration period can vary up to about $(M-1).64$ μs, where M is the number of lines of the photosensitive zone.

The embodiment of FIG. 1 can readily be adapted to line-transfer devices in which the two sequences of removal of the parasitic charges and of reading of the signal charges do not take place during the line return interval. It is only necessary to modify thd drive signals.

The method in accordance with the invention is applicable in the same manner when the photosensitive points consist of photodiodes. The only difference in the case of photodiodes is that the voltages Vref and V_{AC} are not applied to the MOS-phototransistors but to gates which control the transfer between the photodiodes and the columns and which are not exposed to the radiation. When the photodiodes are fabricated on a P-type substrate, the voltage Vref which is applied to the gates and initiates reading of the photodiodes is higher than the voltage V_{AC} which is applied to the gates and permits integration of the charges.

It will clearly be understood that the invention is readily applicable to photosensitive points formed on an N-type substrate.

What is claimed is:

1. A device for modulating the sensitivity of a line-transfer photosensitive device having a photosensitive zone constituted by M lines of N photosensitive points, the photosensitive points of the different lines being connected in parallel by conductive columns to a memory which has the function of transferring signal charges coming from a line of photosensitive points to a read register and of transferring to an evacuation drain parasitic charges which are present in the columns prior to arrival of the signal charges, wherein said device comprises first and second means having the following functions:

the first means carry out a first reading operation of each line when the parasitic charges derived from the columns are transferred from the memory to the evacuation drain so that charges resulting from the first reading operation are consequently removed to the drain at the same time as said parasitic charges;

after an adjustable time interval, the second means carry out a second reading operation of each line when signal charges derived from the columns are transferred from the memory into the read register so that said signal charges resulting from the second reading operation are consequently transferred to the read register and wherein the first and the second means comprise a first and a second shift registers, with M stages, said shift registers being controlled by the same addressing signals, in which said M stages address the M lines of the photosensitive zone via transistors, a drive pulse being applied to the input of each register and said drive pulse being transferred periodically from one stage to the next and wherein modulation of the time interval which elapsed between the first and the second reading of the same line is obtained by varying the time interval which elapses between injection of said drive pulse into each register.

2. A device according to claim 1 wherein the first means comprise two series of M transistors of the MOS type; each MOS transistor having a drain, a source and a gate;

the transistors of one of the series are enhancement-mode MOS transistors connected by their drain and their source to one line of the photosensitive zone and to a bias voltage which permits transfer of charges from the photosensitive points to the columns, the gates of said transistors being connected to one stage of the shift register, the arrival of a pulse in a stage providing reading of the line addressed by said stage;

the transistors of the other series are depletion-mode MOS transistors mounted as emitter-followers, said transistors being connected by their drain and their source to one line of the photosensitive zone and to a bias voltage which permits integration of the charges in the photosensitive points, the departure of a pulse from one stage initiating the integration period of the line which is addressed by said stage.

3. A device according to claim 1 wherein the second means aforesaid comprise a first and a second series of M enhancement-mode MOS transistors, each MOS transistor having a drain, a source and a gate:

the transistors of a first series are connected by their drain and their source to one line of the photosensitive zone and to a bias voltage which permits transfer of the charges of the photosensitive points to the columns, the gates of said transistors being connected to a transistor of the other series;

the transistors of a second series are connected by their drain and their source to a clock signal which indicates the time interval during which the charges derived from the columns are transferred into the read register by the memory and to the gates of transistors of the first series, the gates of said transistors of the second series being each

connected to one stage of the shift register of the second means, each transistor of the second series which is connected to one stage being triggered into conduction by the arrival of a pulse on its stage when the charges derived from the columns are transferred, from the memory into the read register the conduction of said transistor initiating conduction of the corresponding transistor of the first series and therefore reading of one line of the photosensitive zone.

4. A device according to claim 2, wherein the second means comprise a first and a second series of M enhancement-mode MOS transistors, each MOS transistor having a drain, a source and a gate:

the transistors of a first series are connected by their drains and their sources to one line of the photosensitive zone and to a bias voltage which permits transfer of charges from the photosensitive points to the columns, the gates of said transistors being connected to one transistor of the other series;

the transistors of a second series are connected by their drain and their source to a clock signal which indicates the time interval during which the charges derived from the columns are transferred into the read register by the memory and to the gates of transistors of the first series, the gates of said transistors of the second series being connected to one stage of the shift register of the second means, the transistor of the second series which is connected to a given stage being triggered into conduction by the arrival of a pulse on the stage aforesaid when the charges derived from the columns are transferred from the memory into the read register the conduction of said transistor initiating conduction of the corresponding transistor of the first series and therefore reading of one line of the photosensitive zone.

5. A device according to claim 1, wherein the shift registers aforesaid are constituted by MOS transistors.

6. A device according to claim 2, wherein the shift registers aforesaid are constituted by MOS transistors.

7. A device according to claim 3, wherein the shift registers aforesaid are constituted by MOS transistors.

8. A device according to claim 4, wherein the shift registers aforesaid are constituted by MOS transistors.

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